DDRAM

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Dir.Memoria | Descripción | Bit 0 | Bit 1 | Bit 2 |
| La da sysfs | Base address (samples) |  |  |  |
| 0x1e8480 (2,000,000 bytes) | Size (samples) |  |  |  |
|  |  |  |  |  |
|  |  |  |  |  |

PRU1/mem (Clock)

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| --- | --- | --- | --- | --- |
|  |  | Bit 0 | Bit 1 |  |
| 0x00000000 | Delay clock |  |  |  |
| 0x00000004 | Counter | Turn on(1)/off(0) | Update delay value (1) |  |

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| --- | --- | --- | --- | --- | --- |
| Registro | Descripción |  | Bit 0 | Bit 1 | Bit 2 |
| 0x00002000 | Clock Frequency |  |  |  |  |
| 0x00002004 | Clock Running flag |  | turned on/off or updated from Linux userspace | Same as bit 0 |  |
| r30 |  |  |  | Sample clock signal, low(0) |  |
| r0 | delay r2 (50% duty cycle) |  |  |  |  |
| r1 | 0x00000000(delay clock) |  |  |  |  |
| r2 | Clock delay |  |  |  |  |
| r3 | State(load) r1, 4, 4 |  |  |  |  |
| r4 | 0x00010000 |  |  |  |  |
| r5 | | Clock state(aka Sample clock) i.e. high/low |  |  |  |  |

PRU0 (spi con ads1198)

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| --- | --- | --- | --- | --- | --- | --- | --- |
| Registro/mem | Descripción | Bit 0 | Bit 1 | Bit 2 | Bit 3 | Bit 4 | Bit 5 |
| 0x00000000 | SPI Command String |  |  |  |  |  |  |
| 0x00000004 | DDR Base Address |  |  |  |  |  |  |
| 0x00000008 | DDR Size |  |  |  |  |  |  |
| r30 | SPI Lines |  | MOSI (P9\_29) | CLK (P9\_30) | MISO (P9\_28) |  | CS (P9\_27) (0=active low) (1=end of sample) |
| r31 | notification of program completion |  |  |  |  |  |  |
| r0 | SYSCFG reg (load C4,4,4) |  |  |  |  | 0=STANDBY\_INIT |  |
| r1 | 0x00000000 |  |  |  |  |  |  |
| r2 | ADS States (need 16 msb) |  |  |  |  |  |  |
| r3 | 0x00000000 (ADS response data) |  |  |  |  |  |  |
| r4 | Counter (to count the reading/writing of 24 bits(3 bytes) |  |  |  |  |  |  |
| r5 | Clock flag ( 0x00010000) | Clock flag (when high->take a sample) |  |  |  |  |  |
| r6 | Sample clock |  |  |  |  |  |  |
| r7 | 0x000003FF (the bit mask to use on the returned data (i.e., keep 10 LSBs only) |  |  |  |  |  |  |
| r8 | Linux address to store sample values |  |  |  |  |  |  |
| r9 | Size(number of samples to take) |  |  |  |  |  |  |
| r29 | r29.w2 // set a non-default CALL/RET register |  |  |  |  |  |  |

PRU Shared memory (clock samples) (between both PRUs)

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Mem | Descripción | Bit 0 |  |  |
| 0x00010000 | Sample Clock |  |  |  |